REMARKS/ARGUMENTS

Claims 1-28 are pending in the present application. Claims 1, 11, 14, and 21 have been amended. No new matter has been added to the amended claims. Reconsideration of the claims is respectfully requested.

Specification

The specification has been amended to correct typographical errors. No new matter has been added by these corrections.

Claim Rejections - 35 USC § 102

Claims 1-28 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,719,369 to Asano *et al.* (hereafter Asano). The Applicants respectfully disagree with the grounds for these rejections.

Asano

Asano appears to disclose an output circuit comprising an output transistor circuit for applying an output signal to a transmission line. The output circuit of Asano "compensates for the variations in output resistance against the production variations of the element or variations in power supply voltage or temperature in order that a signal of about a half amplitude of the output signal may be always applied to the transmission line when the transmission line is connected to the output circuit to switch the output signal." (Asano at col. 1, lines 59-66).

Fig. 1 of Asano details the structure of the output transistor circuit. The circuit contains output transistors 1 and 6, connected in parallel with transistors 2-5 and 7-10, respectively. Transistors 2-5 and 7-10 are designed for "trimming the gate width" of their respective output transistor. (Asano at col. 2, lines 60-61). It can be shown that the presence of output transistors 1 and 6 results in the output circuit only providing for a decrease in resistance in response to circuit inputs.

For example, considering Fig. 1 of Asano, if the signal applied to inverter 11 is low, P channel MOS transistor 1 will have a high signal at its gate and will be off. Transistors 2-5 are off when the outputs of NAND gates 12-15 are HIGH. When transistor 1 is ON, the

resistance of the output circuit can only decrease when transistors 2-5 turn ON, because transistors 2-5 are connected in parallel with transistor 1. (Asano at col. 3, lines 29-38).

Complementary arguments can be made for N channel MOS transistors 6-10 and NOR circuits 16-19.

Claim 1

Amended claim 1 recites, in part, an impedance matching circuit, "wherein an impedance of the impedance matching circuit increases in response to a change in the values of the digital encoder output signals in a first direction and wherein the impedance of the impedance matching circuit decreases in response to a change in the values of the digital encoder output signals in a second direction." Asano does not teach or suggest these features of claim 1.

As discussed above, Asano discloses a circuit in which the presence of output transistors 1 and 6 regulate the output circuit. In Asano, the transistor gate width can only be trimmed in manner that causes a decrease in the impedance of the output circuit.

The claimed invention, on the other hand, can increase and decrease the impedance of the impedance matching circuit in response to changes in the values of the output signals from the digital encoder circuit.

Claims 2-10

Claims 2-10, which depend from claim 1, are believed to be patently distinct from the cited reference for at least the reasons given above and for the additional limitations they recite. Therefore, the Applicants respectfully submit that claims 2-10 are in a condition for allowance.

Claim 11

Amended claim 11 recites, in part, "setting an impedance of the impedance matching circuit in response to the plurality of second signals, wherein the impedance matching circuit is part of the integrated circuit and the impedance of the impedance matching circuit increases in response to a first condition of the plurality of second signals and decreases in

response to a second condition of the plurality of second signals." As discussed above, the present invention can increase and decrease the impedance of the impedance matching circuit.

This is a feature that is not disclose in or suggested by Asano. Asano can only decrease the impedance. For at least these reasons, amended claim 11 is believed to be in a condition for allowance.

Claims 12-20

Claims 12-20, which depend from claim 11, are believed to be patently distinct from the cited reference for at least the reasons given above and for the additional limitations they recite. Therefore, the Applicants respectfully submit that claims 12-20 are in a condition for allowance.

Claim 21

Amended claim 21 recites, in part, "an impedance matching circuit comprising a plurality of second transistors, wherein each of the second transistors is coupled to receive one of the digital signals, wherein a first state of the digital signals results in an increase in a resistance of the impedance matching circuit and a second state of the digital signals results in a decrease in the resistance of the impedance matching circuit."

As discussed above, these features are not present in Asano. Asano can only a decrease the impedance. For at least these reasons, and others, amended claim 21 is believed to be in a condition for allowance.

Claims 22-28

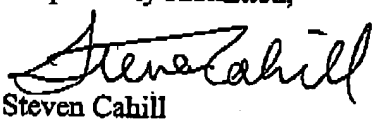
Claims 22-28, which depend from claim 21, are believed to be patently distinct from the cited reference for at least the reasons given above and for the additional limitations they recite. Therefore, the Applicants respectfully submit that claims 22-28 are in a condition for allowance.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



Steven Cahill
Reg. No. 44,578

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 415-576-0300

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